REMARKS

Claims 1-21 remain pending in the application. Claims 1, 15, 18 and 20 have been amended. Claims 2 and 5 have been canceled. Claim 21 has been added

The Office Action states "Listing of references is not a proper information disclosure statement .....and must submitted in a separate paper".

Applicants submit that they had not provided the Examiner with an IDS at the time of filing of the application. An IDS in full compliance with MPEP § 609.04(a) was filed on January 25, 2006, providing a listing of not only all the patents but also the publications referred in the specification, alongside with a copy thereof. The latter were not available at the time of filing the application.

The Office Action states that 'the Declaration is defective because the second inventor has not been signed.'

In response, Applicants enclose herein a copy of the declaration as filed. As it may be determined, a page 2 of the declaration showing only 2 out of 3 signatures, was erroneously incorporated alongside with the correct page 2 that contains all the three inventor's signature. In view of the foregoing, Applicants respectfully request that the erroneous page of the Declaration be discarded, leaving only the second page containing all the three signatures remain.

Accordingly, Applicants contend that the Declaration as originally filed is in full compliance with 37 C.F.R. 1.67(a), and respectfully request that a statement to that effect be provided by the Examiner.

Claim 15 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Applicants have now amended claim 15 as suggested by the Examiner.

Accordingly, Applicants submit that claim 15 as amended is free of rejection under 35 U.S.C. §112, second paragraph, and respectfully request that the Examiner withdraw the rejection of the stated claims based thereon.

Claims 1 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chang et al. (USP 6,415,426) (Chang).

Applicants respectfully traverse this assertion for the following reasons:

1) Chang defines target zones which provide indications of the timing impact of functional cell movement. A detailed search for improved cell placements is conducted in which target zones are used to assess the signal timing impact of proposed cell movements.

In contradistinction, the physical regions as taught by Applicants are defined in order to model the movement of a plurality of cells across the chip simultaneously in two-dimensions to minimize the cell movement during overlap resolution.

2) Chang teaches that each candidate cell that is moved into its target zone during detailed placement be legalized individually by moving and squeezing other cells in the zone to accommodate the candidate cell. Detailed search iteration is completed when the proposed placement of every cell in the design has been evaluated.

Applicants, on the other hand, model the movement of a plurality of cells simultaneously both across the chip as well as within each physical region.

3) Chang teaches that the detailed placement process moves the cells significantly far from its initial location (placement) based on timing impact to the design.

In contrast, Applicants teach how to minimize the placement perturbation while arriving at an overlap free-placement.

In view of the foregoing amendment and arguments, Applicants believe that claims 1 and 20 as amended are free of rejection under 35 U.S.C § 102(b) over Chang (USP 6,415,426), and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claims 1-5 and 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Donelly et al. (USP 6,948,143) (Donelly).

Applicants respectfully traverse the above rejection for the following reasons:

Applicants teach that the physical region definition of the placement-view, the graph model of the neighboring physical regions capture the movement of cells in two-dimensions simultaneously and hence minimizes the total cell movement with respect to initial placement with cell overlaps during placement legalization.

Thus, Donelly teaches away from what Applicants deem to be their invention, namely, that the placement overlap in the X and Y dimensions must be resolved independently. Since Applicants require that the neighboring physical regions capture the movement of cells in two-dimensions simultaneously, it is not possible for Donelly to anticipate Applicant's claims 1-5 and 20, as stated in the Office Action.

In view of the foregoing amendment and arguments, Applicants believe that claims 1-5 and 20 are free of rejection under 35 U.S.C § 102(e) over Donelly (USP 6,984,143), and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claims 6-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Donelly et al. (USP 6,948,143) (Donelly) in view of Dasasathyan et. al. (USP 6,857,115) (Dasasathyan).

Applicants respectfully traverse the above rejection for the following reasons:

Dasasathayan teaches an application of network flow techniques (known optimization methods) to solve local cell placement assignment subject to proximity (shape) constraints. (original) He further teaches an iterative scheme to solve this assignment (matching) problem to obtain a physically realizable solution (overlap-free and satisfies the shape restrictions). A network flow based optimization with constraints reassigns the placement of tristate buffers locally between rows to satisfy the placement constraints. (original) The overlap-free assignment within a row is then achieved as a separate step.

In contrast, Applicants teach a general placement overlap resolution method using network flow techniques that allows movement of plurality of cells in two-dimensions (inter- and intra- circuit rows) simultaneously. Dasasathyan teaches away from the Applicants by teaching a network flow model as an assignment (matching) problem which does not capture the cell area during assignment, while Applicants teach a solution that captures the cell-area both during the global cell-area migration across the integrated circuit as well as during cell movement between physically neighboring regions.

The combination of Donelly of Dasasathyan teaches away from what Applicants deem to be their invention, namely, that the placement overlap in the X and Y dimensions must be resolved independently. Applicants require that the neighboring physical regions capture the movement of cells in two-dimensions simultaneously; thus, it is not possible for Donelly in combination Dasasathayan to render Applicant's claims 6-19 unpatentable, as stated in the Office Action.

It is not even possible that the combination of Donelly and Dasasathayan achieve what Applicants teach, namely that a general placement overlap resolution method using network flow techniques allow the movement of cells in two-dimensions simultaneously.

Regarding the cited reference of USP 6,779,169 issued to Singh et al. which describes a method and apparatus to place components onto programmable logic devices, Applicants submit that Singh et al. teach a global placement of cells in programmable devices, and as such, is not directly applicable to the placement overlap resolution taught by Applicants.

In view of the foregoing, it is respectfully requested that all the outstanding objections and rejections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,
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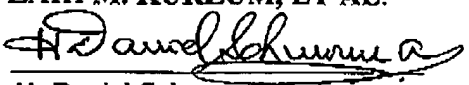
By: 

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